Qualification Test Method and Acceptance Criteria

The summary shown in following tables give brief descriptions of the various reliability tests. Not all of the tests listed are performed on each product and other tests can be performed when appropriate.

Table 1: Qualification Test Method and Acceptance

	Test item	Applied with	Test method	Test condition	Sample #(Min)	Acc No	Comments
1	High Temp. Operating Life (HTOL)	All ISSI products.	JEDEC 22 A108 MIL-STD-883 1005	T=125℃, Apply Voltage ≧1.1Vcc, Dynamic	77	0	Acceptable number is upon sample size. For Memory: Target failure rate < 100 FITs at 60% CL after 1 Khrs.
2	Electrostatic Discharge (ESD)	All ISSI products.	ANSI/ESDA/JEDEC JS-001 ANSI/ESDA/JEDEC JS-002	Human Body Model (HBM) R=1.5kohm, C=100pF. Charge Device Model (CDM).	3 HBM 3 CDM	0 0	3samples for each test mode HBM ≧ ±2000V. CDM≧±500V (corner pins >= ±750V) for SRAM/DRAM Automotive devices 3pcs for each voltage level for Analog
3	Latch-up	All ISSI products.	JEDEC STD No. 78	Current trigger Voltage trigger	3 3	0 0	(I trigger) ≧ ± 100 mA (V trigger) ≧ + 1.5x Vcc or MSV, which is less.
4	Infant Mortality	DRAM / SRAM		T=125℃, Vcc applied upon device types, Dynamic.	1300	Optional	Target failure rate < 100 FITs after 96 hrs at 60% CL.
5	Soft Error	≧1M DRAM / SRAM	MIL-STD-883 1032 JEDEC 89	Source: Alpha particle Am-241, test patterns: checker board or reverse checkerboard at room temp.	3	< 1K FITs	Target failure rate < 1000 FITs/Mbit at 60% CL.
6	High Temp. Storage	All ISSI products	JEDEC 22 A103 MIL-STD-883 1008 JEDEC22-A117	T=150℃, 1000hrs	45	0	** S/S=77ea for Flash/pFusion.
7	Highly Accelerated Stress Test (HAST)	All ISSI products .	JEDEC 22 A110	T=130℃, 85%RH, 33.3 psia, Apply Voltage=1.1VCC,	25	0	Use LTPD 10% For Analog:

				96hrs min.(or T=110 ℃, 85%RH, 17.7psia , Apply Voltage=1.1xVCC, 264 hrs)			S/S=77ea Use LTPD=5%, no failure is allowed.
8	Autoclave (Pressure Cooker, PCT)	Non BGA pkg types	JEDEC 22 A102	T=121℃, 100%RH, 30psia 168 hrs	25	0	Use LTPD 10% For Analog: S/S=77ea Use LTPD=5%, no failure is allowed.
9	Temperature Cycling	All pkg types	JEDEC 22 A104 MIL-STD-883 1010	T=-65℃ to 150℃, dwell time=15min, Temperature transition time =15 min 250 cycles (Or equivalent -55C to 125℃, 700-1000 cycles)	25	1). 0	Use LTPD 10% For Analog: S/S=77ea Use LTPD=5%, no failure is allowed.
10	Pre-conditioning	All pkg types	JEDEC 22 A113	Bake 24hrs @+125℃, moisture soak (level 3: 192 hrs@30℃ /60%RH), reflow solder IR @ (a) For non Pb-free: 240+5/-0℃, (b) For Pb-free: 260 +5/-0℃,	77	1	Use LTPD 5%. The parts, passed level 3 test, will be used to do HAST, T/C, PCT. Level 1 & 2 are optional. S/S=231ea for Analog.
11	Physical Dimensions	All pkg types	JEDEC 22 B100 MIL-STD-883 2016		30	0	Cpk≧1.67
12	Solderability	only for L/F package	J-STD-002	1. Steam aging - Temp : 93+3/-3℃, Time : 8±0.25 hrs. (Optional) 2. For non Pb-free T=215±5℃, and For Pb-free T=245±5℃, Dwell time = 5±0.5sec,	15	0	Lead coverage area > 95%

13	IR Reflow Soldering	only for substrate package	J-STD-002	1. Stam aging - Temp : 93+3/-3℃, Time : 8±0.25 hrs. (Optional) 2. Reflow Temp: a.Pb-free: 230~250℃ b.SnPb: 215~230℃	15	0	Use LTPD=15%. No failure is allowed.
14	Lead Integrity	For through-hole devices only	JEDEC 22-B105 MIL-STD-883 2004	1) 2 oz for SOJ and TSOP, 8 oz for other Pkg 2) for bending arc = 90 ±5 degree 3) 2 cycles for TSOP, 3 cycles for other Pkg	45 leads of 5	0	No failure
15	Mark Permanency	All pkg (ink marking) except BGA (Laser Marking)	JEDEC 22 B107 MIL-STD-883 2015		5	0	Use LTPD 50%
16	Wire Bond Strength	Option to all pkgs	MIL-STD-883 2011		30 bonds of 5	0	Ppk≧1.66 or Cpk≧1.33 Strength≧ 3gram For all product, Bond pull SPEC has depend on wire diameter,
17	Die Bond Strength	Option to all pkgs	MIL-STD-883 2011		5	0	Bond shear strength not less than 30 gram.
18	Scanning Acoustic (SAM) Microscope Inspection	For new assembly process, package	Criteria based on new assembly process and package specification	1) Die surface 2) Interface of die and die attach material 3) Interface of lead frame pad and mold	9(3 each from HAST, T/C, PCT)	0	Before IR-Reflow, 0% delamination on die surface and <10% at the lead finger area. After IR-Reflow, <30% on die surface and <50% at lead finger area.
19	Co-planarity	Only for SMD pkg	JEDEC 22 B108	Measured accuracies within ± 10% of specified deviation	5	0	Failure specification. Deviation=4 mil.
20	Solder Ball Shear	Substrate type package	JEDEC 47	50 balls of 10	0	1	Ppk>=1.66 or Cpk>=1.33

Table2 : Qualification Test Method and Acceptance Criteria (Nonvolatile memory portion)

	Qualification Test	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments
1	Endurance Cycle	JEDEC22-A117	1) T=85℃/25℃ 2) V=Vcc Max 3) Cycling 100K for Flash and 10K for pFusion.[*1] (MTP: 20K)[*1]	39/38	0[*2]	3	For Flash and eFusion. (Not apply to OTP).
2	HTDR(Data retention after Cycling)	JESD47 JEDEC22-A117	1) T=125℃ 2) 10/100hrs	39	0[*2]	3	For Flash and pFusion only (Not apply to OTP)
3	LTDR(Read stress after cycling)	JESD47 JEDEC22-A117	1) T=Room temp 2) 500hrs	38	0[*2]	3	For Flash and pFusion only (Not apply to OTP)

[*1] Specific cycling SPEC refers to product datasheet.

[*2] A/R: the reject criteria maybe different from case to case per the discussion with foundry for eFusion.

Table3 : Test upon request or optional test

	Qualification Test	Applied to	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments
1	Resistance to Solder Heat	option to all pkgs	JEDEC 22 B106 MIL-STD-750 2031	T=260±5℃ t=10+2/-0 sec. lead immersion is 0.05”.	5	0	1	Package related test.
2	Salt Atmosphere	option to all pkgs	MIL-STD-883 1009	T=35℃, 5% NaCl t=24hrs	5	0	1	Package related test.
3	Pressurizing body	option to all pkgs	EIAJ ED4702	Load: 10N Time: 10±1sec Pressurizing jig : R0.3cm	22	0	1	Criteria: F/T test
4	Vibration	option to all pkgs	JESD22-B103	Frequency : 20 ~ 2000Hz Acceleration : 20G peak Displacement : 1.52mm Sweep time : 20 ~ 2000 ~ 20Hz in 4 mins Duration : 4 times per X,Y,Z axis, Total : 48 mins	11	0	1	Criteria: F/T test

Table4 : Level 2 / Board level test (Selective)

	Qualification Test	Test Method	Test Conditions	Samp. Size	Rej. No.	Lots Req.	Comments	Note
1	Bending	IPC-JEDEC-9702	1) Daisy-Chain package 2) Travel speed: 1~1.42mm/sec which depends on board thickness 3) Strain rate : >5,000µstrain/sec 4) Give weibull slope	22	0	1	20% change in resistance	By request
2	Shock (Drop Test)	JESD22-B111	1) Daisy-Chain package 2) Use event detector 3) 3 shock for each top and bottom face 4) 340 G For hand product: 5) 30 shock for 4 face 6) 1500G, half-sine	15 per board	0	1	10% change in resistance	By request
3	Solder Joint Life Test	IPC-JEDEC-9701	1) Daisy-Chain package 2) T= -0 to 100℃ Hand product: T= -40 to 125℃ 3) Temp slope= 10 ℃/ min, Dwell T= 10 min 4) Real-Time Measurement	32 virgin + 10 rework	0	1	20% change in resistance Pass 3500 cycles 32 (Virgin sample) and 10 (Rework sample)	By request
4	Solder Joint Strength	IPC-JEDEC-9701	1) T=-0 to 100℃. 2) Temp slope= 10℃/ min, Dwell T= 10 min 3) Pull test	5	0	1	Pass 3500 cycles Bond pull strength not less than 3 gram	By request

The qualification for automotive application should follow the requirements of AEC-Q100. The test items of reliability qualification for automotive are shown as following:

Table5 : Automotive Qualification Test Method and Acceptance Criteria (device portion)

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
HTOL (High Temp. Operating Life)	AEC-Q100#B1	JESD22A108	77 X 3 lots	0 fail	Grade 1 : T=125℃, 1000 hrs.Vcc max operating for both DC /AC parameter. F/T check before and after at low, and high temp. Should do Cycling test before HTOL for Flash/pFusion.
ELFR (Early Life Failure Rate)	AEC-Q100-008	JESD22A108	800 X 3 lots	0 fail	Grade 1 : T=125℃, 48 hrs.Vcc max operating for both DC /AC parameter. F/T check before and after at low, and high temp.
HTSL (High Temp. Storage Life)	AEC-Q100#A6	JESD22A103	45 X 3 lot **	0 fail	Grade 2 : 150℃, 1000 hrs. F/T check before and after at high temp. **Should do cycling test before HTSL with S/S=77ea if it's for cover HTDR for Flash/pFusion.
SER (Soft Error Rate)	AEC-Q100#E11	JESD89-1,-2,-3	3 X 1 lot	< 1k FITs/Mbit	For devices with memory sizes >= 1 Mbits SRAM or DRAM based cells.
Endurance Cycle	AEC-Q100-005	JEDEC22-A117	77 x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=85℃/25℃ 2) V=Vcc Max 3) Cycling 100K for Flash and 10K for pFusion.* (MTP: 20K)
HTDR (High Temperature Data Retention)	AEC-Q100-005	JEDEC22-A117	77 x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=150℃ 2) 10/100hrs. Remark: HTDR can be covered by cycling+HTSL.

LTDR (Low Temperature Data Retention Storage Life)	AEC-Q100-005	JEDEC22-A117	77x 3 lots	0 fail	For Flash and pFusion.(Not apply to OTP). 1) T=Room temp storage 2) 1000hrs

*Remark: Some specific devices with different cycling count SPEC should follow the statement in the datasheet.

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
ESD HBM	AEC-Q100-002	ANSI/ESDA/JEDEC JS-001	3 devices for each step X 1 lot	±2 kV	F/T check before and after at high temp (IV curve check for every 500V)
ESD CDM	AEC-Q100-011	ANSI/ESDA/JEDEC JS-002	3 devices for each step X 1 lot	±500 V (corner pins ≧ ±750V)	F/T check before and after at high temp (IV curve check)
Latch-up	AEC-Q100-004	JESD78	6 devices X 1 lot	±100mA +1.5 X max Vcc or MSV, which is less	F/T check before and after at high temp (Icc variation check for initial and F/T check for final confirm)

Table 6 : Automotive Qualification Test Method and Acceptance Criteria (package portion)

Test Item	Reference Doc.	Test Method	Sample size / lot (Minimum)	Accept Criteria	Notes
Preconditioning	AEC-Q100#A1	JESD22A113	231 X 3lots	0 fail	Level 3. Prior to TCT, PCT, THB. F/T check before and after at room temp. Delam. on die surface is acceptable if can pass subsequent tests.
TCT (temp cycling)	AEC-Q100#A4	JESD22A104	77 X 3 lots	0 fail	Grade 1 : -65~150℃, 500 cycles. (Or equivalent -55~125℃, 1000 cycles) F/T check before and after at high temp
PCT (autoclave or pressure cooker)	AEC-Q100#A3	JESD22A102	77 X 3 lots	0 fail	121℃/30psia/100%RH. a.168 hrs for LF type, b.It’s not applied for laminate based packages. F/T check before and after at room temp
THB (temp humidity bias or HAST)	AEC-Q100#A2	JESD22A101, JESD22A110	77 X 3 lots	0 fail	THB: 85℃/85%RH/1000 hrs with bias HAST: 130℃/85%RH/Minimum 96 hrs with bias (or 110℃/85%RH/264 hrs) F/T check before and after at high temp